## REMARKS

Claims 34 and 36 are amended. Claim 35 is canceled. No claims are newly added. Accordingly, after entry of this Amendment, claims 1-34 and 36-65 will remain pending. Claims 1-33 have been withdrawn from further consideration by the Examiner. Accordingly, claims 34 and 36-65 are currently under examination.

In the Office Action dated January 10, 2006, the Examiner acknowledged the Applicant's traverse of claims 34-65 in the reply filed on December 5, 2006. The Examiner did not accept the traversal and made the Restriction Requirement final. While the Applicant respectfully disagrees with the Examiner's determination, the Applicant acknowledges the Examiner's decision.

In the Office Action, the Examiner rejected claims 34-44, 46-49, 51-62, and 64-65 under 35 U.S.C. § 102(b) as being anticipated by Kagoshima et al. (U.S. Patent Application Publication No. 2003/0003607). Claims 45, 50, and 63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kagoshima et al. in view of Gardner et al. (U.S. Patent No. 6,087,238). The Applicant respectfully disagrees with the Examiner's rejections and, therefore, respectfully traverses the same.

Claims 34 and 36-65 recite a processing tool that combines a number of features including, among them, at least one processing system configured for performing a trimming process on the gate electrode structure to form a trimmed dimension and for repeating the performing of the trimming process on the gate electrode structure at least once until a target trimmed dimension is obtained. Neither of the references, either alone or in combination, disclose or suggest such a combination. Accordingly, the Applicant respectfully submits that claims 34 and 36-65 are patentable thereover.

Before addressing the references directly, the Applicant acknowledges the Examiner's statement on page 3 of the Office Action that claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than by function. While the Applicant does not disagree with the Examiner's recitation of the case law, the Applicant respectfully submits that the recitation of qualifying language may assist in defining the structure of an apparatus, as in this case.

As used in the claims, the term "processing system" is very broad. To assist the Examiner to distinguish the processing system recited by the present claims from processing systems in the prior art, the Applicant has employed language related to the operation of the processing system. While the language is functional, the

Applicant respectfully submits that the language is not purely a definition of function of the processing system. The language has been employed to define the structure recited by the claims. The Applicant respectfully submits, therefore, that the Examiner should consider the language in the claims in determining the patentability of the claims 34 and 36-65.

With this in mind, the Applicant respectfully submits that Kagoshima et al. cannot be relied upon to anticipate any of claims 34 and 36-65. Kagoshima et al. describes a disturbance-free, recipe controlled plasma processing system and method. Specifically, Kagoshima et al. describes a plasma processor 1 that generates a plasma. (Kagoshima et al. at paragraph [0027].) The operation of the plasma processor 1 is described in paragraph [0033], as follows:

> When completing etching operation corresponding to a single wafer in a step 7, the system estimates a processed result of the wafer on the basis of the measured values of the in-situ sensors and with use of the processed-result estimation model in a step 8. In a step 9, the system corrects the optimum recipe calculation model on the basis of the estimated processed result and target value as shown in FIG. 4, and sets the corrected optimum recipe for the plasma etcher 23. The system then proceeds to the step 2 for processing the next wafer.

(Kagoshima et al. at paragraph [0033], emphasis added.) As the foregoing discussion makes abundantly clear, the system described by Kagoshima et al. processes each wafer only once before proceeding to the next wafer. Accordingly, the system described by Kagoshima et al. does not include, among other features, at least one processing system configured for performing a trimming process on the gate electrode structure to form a trimmed dimension and for repeating the performing of the trimming process on the gate electrode structure at least once until a target trimmed dimension is obtained. As a result, the Applicant respectfully submits that Kagoshima et al. cannot be relied upon to render obvious any of claims 34 and 36-65.

Gardner et al. does not assist the Examiner with a rejection of the claims under 35 U.S.C. § 103(a) because Gardner et al. is similarly deficient. Gardner et al. describes a semiconductor device having a reduced-width polysilicon gate and non-oxidizing barrier layer and method of manufacture thereof. There is no discussion of any semiconductor processing equipment. Accordingly, Gardner et al. also does not discuss or suggest a processing tool that includes, among other features, at least one

processing system configured for performing a trimming process on the gate electrode structure to form a trimmed dimension and for repeating the performing of the trimming process on the gate electrode structure at least once until a target trimmed dimension is obtained. As a result, the Applicant respectfully submits that Gardner et al. cannot be combined properly with Kagoshima et al. to render obvious any of claims 34 and 36-65.

Each of the rejections having been addressed, the Applicant respectfully submits that claims 34 and 36-65 are in a condition for allowance and such is respectfully requested.

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Respectfully submitted,

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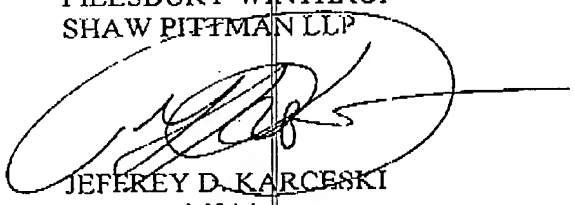

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